# PATENT ABSTRACTS OF JAPAN

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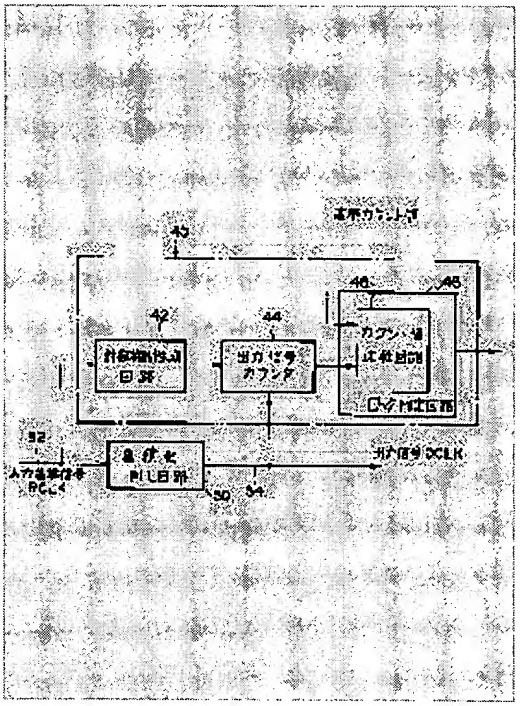
## (54) PHASE LOCK DETECTING CIRCUIT

(57)Abstract:

PROBLEM TO BE SOLVED: To attain phase lock detection for a PLL circuit which is packaged into one from which the inside intermediate generation signal cannot be extracted.

SOLUTION: An input reference signal 32 to an integrated PLL circuit 30 is inputted to a counting period generating circuit 42, and a counting period signal pulse having pulse length which is prescribed times as long as the cycle is generated synchronously with this. An output signal counter 44 uses this counting period signal pulse as an enable signal, and counts the number of waves of an output signal 34, outputted from the integrated PLL circuit 30 in the pulse period. A reference count value which is preliminarily decided based on the design values of the time length of the counting period signal pulse and a frequency conversion rate in the integrated PLL circuit 30 is set in a count value comparator circuit 48. A lock-judging circuit 46 judges the state of the phase lock between the input and output signals of the integrated PLL circuit 30 from the size of the reference count value and an output count value measured by the output signal counter 44.




LEGAL STATUS

JP10322200

## DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention is used for the phase-locked loop circuit which outputs the output signal changed into a different frequency from an input-reference signal, and relates to the phase lock detector which detects the lock of the phase simulation between an input-reference signal and an output signal.
[0002]
[Description of the Prior Art] Drawing 3 is the block block diagram of the phase-locked loop (PLL:Phase Locked Loop) circuit 2 known conventionally. Dividing of the input-reference signal RCLK from the outside (it considers as a frequency fR.) is carried out so that it may become the frequency (it considers as a frequency fM.) of 1/M of an input-reference signal with the M counting-down circuit 4. This M dividing signal MCLK is made into the signal for criteria to a phase comparator 6 which is one of the two inputs. The signal for a comparison which is one input which will be accepted to a phase comparator 6 is N dividing signal NCLK (it considers as a frequency fN.) which carried out dividing of the output signal OCLK from the PLL circuit 2 (it considers as a frequency fOUT.) to the frequency of 1-/N with the N counting-down circuit 8.
[0003] M dividing signal according to the reference signal inputted into the PLL circuit 2 and N dividing signal according to the output signal from the PLL circuit 2 are inputted into a phase comparator 6 as criteria and a signal for a comparison, respectively, it detects the phase contrast of both signals, and outputs the error signal according to the phase contrast. The charge pump 10 changes and outputs the error signal from a phase comparator 6 to "H" level and "L" level and three values of high impedance. A low pass filter 12 graduates the output signal of the charge pump 10, and controls a voltage controlled oscillator (VCO:Voltage Controlled Oscillator) 14 by the dc component. VCO14 outputs the signal which changed the oscillation frequency according to the direct current voltage of the output of a low pass filter 12. This signal turns into the output signal OCLK from the PLL circuit 2. Moreover, this output signal OCLK also becomes an input to the N counting-down circuit 8, as mentioned above.
[0004] In addition, especially in the case of M= 1 and N= 1, it is not necessary to form M counting-down circuit and N counting-down circuit, respectively. Therefore, there may also be a configuration of the PLL circuit 2 which does not have the M counting-down circuit 4 or the N counting-down circuit 8.
[0005] Drawing 4 is the block block diagram of the PLL circuit equipped with the conventional phase lock detector. In drawing 4 , the same sign is given to the same component as drawing 3 , and explanation is omitted. With the conventional configuration, M dividing signal MCLK and N dividing signal NCLK which are inputted into a phase comparator 6 are branched, respectively, and the exclusive "or" circuit 20 which considers each [ these ] signal as an input is formed. It is used in order to detect whether a phase has this exclusive "or" circuit 20 in a lock condition, or the phase of M dividing signal MCLK and N dividing signal NCLK has gathered. When the phase of M

dividing signal MCLK and N dividing signal NCLK has shifted, the period when the logical level of both signals differs arises. In this period, an exclusive "or" circuit 20 outputs the signal of "H" level, and, on the other hand, outputs the signal of "L" level to the period whose logical level of both corresponds. Therefore, conventionally, it had the signal of "H" level from an exclusive "or" circuit 20, and lock-off was detected. Furthermore, it measured conventionally using the external clock which has a small period compared with that period from this exclusive "or" circuit 20, the signal period of phase shifts, i.e., amount, of "H" level outputted, and using for control of the circuit using the output of the PLL circuit 2 or the PLL circuit 2 was also performed.

[0006] Incidentally, since loop control acts so that the frequency and phase of both inputs of a phase comparator 6 may be in agreement, the PLL circuit 2 shown in drawing 3 is controlled to become fM=fN, i.e., fR/M=fOUT/N, in a lock condition. That is, an output signal OCLK serves as a frequency which becomes fOUT=N/MxfR, and the signal changed into the signal fR N/M twice the frequency of an input reference is outputted from VCO14. Here, by changing N and M, the signal of various frequencies can be acquired and the circuit which applies this and is called a frequency synthesizer is realized.

[0007]

[Problem(s) to be Solved by the Invention] In the conventional phase lock detector mentioned above, two signals which are inputted into an exclusive "or" circuit 20 and compared with it turn into two signals which are inputted into a phase comparator 6 and compared. Now, in order to attain the miniaturization of the equipment using the PLL circuit 2, there are not few cases where integrate on a semi-conductor substrate, or the whole PLL circuit 2 or the part which contains a phase comparator 6 at least is offered with the gestalt contained in one package, and this is used as components which constitute equipment. In components-izing of such a PLL circuit 2, although a part of range included to the phase lock detector according to the application may be used as elegance, since the need of detecting especially a phase lock is a low application, there are some which are offered as smaller components only in the part which does not include a phase lock detector. however, generally the PLL circuit module constituted so that the phase lock detector of this latter might not be included takes out outside two signals both inputted into a phase comparator 6 -- as -- it is not constituted. Therefore, there was a problem that the conventional phase lock detector could also be prepared by external, and that use range was limited to the PLL circuit module which does not include this phase lock detector.

[0008] Moreover, with the configuration of the phase lock detector using the conventional exclusive "or" circuit 20, when lock-off needed to be evaluated quantitatively, there was also a problem that the external clock whose frequency was stable was needed apart from the clock for actuation of PLL circuit 2 the very thing.

[0009] It was not made in order that this invention might cancel the above-mentioned trouble, and it makes it possible to perform phase lock detection also to the PLL passive circuit elements which do not include a phase lock detector, and aims at offering the phase lock detector which moreover does not need a special external clock.

[0010]

[Means for Solving the Problem] The phase lock detector concerning this invention is used for the phase-locked loop circuit which generates the output signal of the frequency

which has a predetermined frequency-conversion ratio to the frequency of an input-reference signal. The output signal counter which is the phase lock detector which detects the phase lock of the phase-locked loop circuit concerned, and carries out counting of the wave number of said output signal outputted from said phase-locked loop circuit, counting of said output signal counter -- counting which defines a period -- counting which generates a period signal based on said input-reference signal -- with a period generation circuit said frequency-conversion ratio and said counting -- it has the lock judging circuit which judges said phase lock based on the difference between the criteria counted value beforehand defined based on a period, and the output counted value of said output signal counter.

[0011]

[Embodiment of the Invention] Next, the operation gestalt of this invention is explained with reference to a drawing. Drawing 1 is the block diagram of the outline of the frequency synthesizer using PLL which is the gestalt of operation of this invention. The input-reference signal RCLK32 is inputted into the integration PLL circuit 30 constituted including the PLL circuit 2, and it outputs the output signal OCLK34 which has the frequency fOUT which doubled this frequency fR N/M. This integration PLL circuit 30 does not need to have the terminal for taking out the signal in that interior. the phase lock detector 40 concerning this invention -- counting -- it is constituted including the period generation circuit 42, the output signal counter 44, and the lock detector 46. The lock judging circuit 46 includes the counted value comparator circuit 48 which compares the criteria counted value set up beforehand with the output counted value outputted from the output signal counter 44. About a detail of operation, it mentions later using more detailed drawing. Here, only the big description of a basis phase lock detector is explained using drawing 1 . The input-reference signal RCLK32 with which the big description of the phase lock detector 40 is inputted into the integration PLL circuit 30, and the signal generated in-between in the integration PLL circuit 30 interior, using the output signal OCLK34 with which it is finally generated by the integration PLL circuit 30, and is outputted as a main input signal are in the point which is not needed.

[0012] Drawing 2 is the block diagram shown to the block configuration inside the integration PLL circuit 30, in order to explain actuation of the gestalt of this operation. Dividing of the input-reference signal RCLK32 of the frequency fR from the outside is carried out with the M counting-down circuit 64, and M dividing signal MCLK66 which has the frequency fM of 1/M of an input-reference signal is generated.

[0013] Moreover, although the output signal OCLK34 which finally has a frequency fOUT is outputted from the integration PLL circuit 30, this OCLK34 branches in the integration PLL circuit 30 interior, and one of them is inputted into the N counting-down circuit 68. The N counting-down circuit 68 carries out dividing of the OCLK, and generates N dividing signal NCLK70 which has the frequency fN of the 1-/N.

[0014] M dividing signal MCLK66 and N dividing signal NCLK70 which were generated in this way are inputted into a phase comparator 72. PLL controls so that the phase of two input signals to this phase comparator 72 gathers. Incidentally, the conventional phase lock detector mentioned above used the property of this PLL of being controlled to have the frequency and phase with two same inputs to this phase comparator 72. On the other hand, since the phase lock detector 40 does not use this property, it does not need to output MCLK66 or NCLK70 which the integration PLL circuit 30 generates

in that interior.
[0015] A phase comparator 72 detects the phase contrast of MCLK66 and NCLK70 which were inputted, and outputs the error signal according to the phase contrast. The charge pump 74 changes and outputs the error signal from a phase comparator 72 to "H" level and "L" level and three values of high impedance. A low pass filter 76 graduates the output signal of the charge pump 74, and controls VCO78 by the dc component. VCO78 outputs the output signal OCLK which has the oscillation frequency fOUT according to the direct current voltage of the output of a low pass filter 76.
[0016] Since loop control acts so that the frequencies fM and fN of both inputs of a phase comparator 72 may be in agreement as already stated, it is set to fOUT= (N/M) and fR. That is, the signal changed into the signal fR N/M twice the frequency of an input reference is outputted from VCO78, and the frequency synthesizer which can acquire the signal of various frequencies is realized by changing N and M.
[0017] Now, actuation of the phase lock detector 40 is explained below. RCLK32 inputted into the integration PLL circuit 30 branches -- having -- counting of the phase lock detector 40 -- it is inputted into the period generation circuit 42. counting -- the period generation circuit 42 is constituted including a counter, and generates the measurement period signal pulse which has the time amount length WREF which corresponds the predetermined twice of the period based on RCLK. For example, it can be set as WREF=1sec extent to fR=14MHz. This measurement period signal pulse is supplied to the output-signal counter 44 as an enable signal.
[0018] The time amount width of face WREF is set up more greatly than periodic tauOUT of an output signal OCLK. That is, it is set up so that it may become WREF=kOUT-tau OUT (kOUT> 1) by making kOUT into a proportionality constant. Here, the accuracy of measurement improves, so that WREF is so large that [ that is, ] kOUT is large since the accuracy of measurement of the phase shift of tauOUT serves as 2 pi/kOUT [rad] about.
[0019] When a measurement period signal pulse is in enabling state, the output-signal counter 44 counts the wave number of the output signal OCLK inputted from the integration PLL circuit 30, and outputs the counted value (output counted value COUT).
[0020] Output counted value COUT which the output signal counter 44 counted is inputted into the counted value comparator circuit 48 in the lock judging circuit 46. The wave number of the output signal generated between measurement period signal pulse width WREF(s) in the phase lock condition of this integration PLL circuit 30 is beforehand set to the counted value comparator circuit 48 as criteria counted value CREF. The counted value comparator circuit 48 compares this criteria counted value CREF with output counted value COUT actually measured by the output signal counter 44.
[0021] the case of COUT>CREF -- the ratio of the frequency of OCLK, and the frequency of RCLK -- it means that correspond when fOUT/fR is larger than N/M, that is, the phase of OCLK progresses to RCLK. On the other hand, it means that the phase of OCLK is overdue to RCLK in COUT<CREF. In a phase lock condition, frequency-ratio fOUT/fR=N/M is realized and this is distinguished from becoming COUT=CREF. Thus, the counted value comparator circuit 48 can judge the size relation between COUT and CREF, and the lock judging circuit 46 can detect the existence of the phase shift of RCLK and OCLK based on the judgment result. Although this phase shift may always be

produced, a little gap is easily corrected by the loop control by PLL. If the difference between COUT and CREF becomes more than how much, the lock judging circuit 46 will have the conditions of whether to judge with lock-off set up, will perform the judgment of a phase lock condition or a lock OFF state based on the criterion, and it outputs the result.

[0022] If CREF set as the counted value comparator circuit 48 has fixed frequency-ratio N/M, it is good at a predetermined fixed value. However, either of the division ratios M and N of the M counting-down circuit 64 of the integration PLL circuit 30 and the N counting-down circuit 68 is constituted by adjustable, and when frequency-ratio N/M is adjustable, CREF is also changed according to it. This modification can be constituted so that user actuation and frequency-ratio change actuation of the integration PLL circuit 30 may be interlocked with and it may be automatically carried out from the exterior of the phase lock detector 40.

[0023] The value of CREF set as the counted value comparator circuit 48 is given by WREF-fOUT. However, fOUT which appears in this formula is not the actual frequency of OCLK outputted from the integration PLL circuit 30 but that desired value. That is, fOUT here is equivalent to -(N/M) fR. Table 1 is a table showing the example of CREF set to the counted value comparator circuit 48. In a table, the left column is fOUT as a target frequency of the output signal OCLK mentioned above, and the right column is a frequency setting value which is CREF corresponding to each fOUT in the case of being WREF=1sec. This frequency set point CREF is expressed in hexadecimals corresponding to the data format on the memory with which the counted value comparator circuit 48 is equipped.

[Table 1]

| PLL出力信号 | 周波数設定値 (HEX) |
|---|---|
| 10kHz | 2710 (HEX) |
| 100kHz | 186A0 (HEX) |
| 1MHz | F4240 (HEX) |
| 10MHz | 989680 (HEX) |

[0024] now, counting -- since the period generation circuit 42 determines the time amount width of face WREF using the counter which operates synchronizing with RCLK, if the frequency of RCLK is changed, WREF will also interlock and change to it. the actual period to which RCLK may be changed in tauREF here, and kREF -- a proportionality constant, then actual counting -- the time amount width of face of a period signal pulse can be expressed with a degree type.

[0025]

WREF=kREF-tau REF ..... (1)

WREF-fOUT which gives the value of CREF on the other hand as mentioned above is equivalent to a degree type.

[0026]

(N/M) WREF-fR ..... (2)

(2) In a formula, WREF and fR are the actual values which may be changed, respectively. (2) When (1) type is substituted for a formula, WREF is eliminated and it takes into consideration that it is fR=1-/tauREF, as for CREF, it turns out that it is expressed in the format of not being influenced by RCLK of fluctuation, like a degree type.

[0027]
CREF= (N/M) and kREF ..... (3)
That is, it is not dependent on an actual measurement and it turns out that the value of CREF set as the counted value comparator circuit 48 from this is good by the constant called for from the design parameter of a circuit. That is, this equipment is easy to constitute at the point that what is necessary is just to set beforehand CREF which is not influenced by RCLK of fluctuation as the counted value comparator circuit 48, and, moreover, the precision of a judgment of the condition of a phase lock is secured also by such easy configuration.
[0028]
[Effect of the Invention] according to the phase lock detector of this invention -- counting -- a period generation circuit -- the input-reference signal to a PLL circuit -- being based -- counting -- a period signal -- generating -- an output signal counter -- counting -- counting defined by the period signal -- the wave number of the output signal outputted to a period from a PLL circuit is counted. A lock judging circuit judges whether it is a phase lock condition for this output counted value as compared with criteria counted value. That is, the signal inside a PLL circuit generated in-between is not used for a basis phase lock detector at all using the input-reference signal to a PLL circuit, and the output signal outputted as the final result from a PLL circuit. Thereby, the phase lock detector of this invention can be applied also to the integrated PLL circuit, an accurate phase lock detection means is offered to the PLL circuit integrated with the configuration which does not include a phase lock detection means especially in the interior, and the effectiveness of expanding the use range of the PLL circuit is brought about.
[0029] The phase lock detector of this invention not needing the external clock whose frequency's was stable in the actuation, and criteria counted value are beforehand defined based on the design parameter of a PLL circuit etc., by not being dependent on the stability of an input-reference signal, are very easy to constitute and, moreover, effective in it being stable and an accurate phase lock detector being offered.

## TECHNICAL FIELD

[Field of the Invention] This invention is used for the phase-locked loop circuit which outputs the output signal changed into a different frequency from an input-reference signal, and relates to the phase lock detector which detects the lock of the phase simulation between an input-reference signal and an output signal.

## PRIOR ART

[Description of the Prior Art] Drawing 3 is the block block diagram of the phase-locked loop (PLL:Phase Locked Loop) circuit 2 known conventionally. Dividing of the input-reference signal RCLK from the outside (it considers as a frequency fR.) is carried out so that it may become the frequency (it considers as a frequency fM.) of 1/M of an input-

reference signal with the M counting-down circuit 4. This M dividing signal MCLK is made into the signal for criteria to a phase comparator 6 which is one of the two inputs. The signal for a comparison which is one input which will be accepted to a phase comparator 6 is N dividing signal NCLK (it considers as a frequency fN.) which carried out dividing of the output signal OCLK from the PLL circuit 2 (it considers as a frequency fOUT.) to the frequency of 1-/N with the N counting-down circuit 8.

[0003] M dividing signal according to the reference signal inputted into the PLL circuit 2 and N dividing signal according to the output signal from the PLL circuit 2 are inputted into a phase comparator 6 as criteria and a signal for a comparison, respectively, it detects the phase contrast of both signals, and outputs the error signal according to the phase contrast. The charge pump 10 changes and outputs the error signal from a phase comparator 6 to "H" level and "L" level and three values of high impedance. A low pass filter 12 graduates the output signal of the charge pump 10, and controls a voltage controlled oscillator (VCO:Voltage Controlled Oscillator) 14 by the dc component. VCO14 outputs the signal which changed the oscillation frequency according to the direct current voltage of the output of a low pass filter 12. This signal turns into the output signal OCLK from the PLL circuit 2. Moreover, this output signal OCLK also becomes an input to the N counting-down circuit 8, as mentioned above.

[0004] In addition, especially in the case of M= 1 and N= 1, it is not necessary to form M counting-down circuit and N counting-down circuit, respectively. Therefore, there may also be a configuration of the PLL circuit 2 which does not have the M counting-down circuit 4 or the N counting-down circuit 8.

[0005] Drawing 4 is the block block diagram of the PLL circuit equipped with the conventional phase lock detector. In drawing 4 , the same sign is given to the same component as drawing 3 , and explanation is omitted. With the conventional configuration, M dividing signal MCLK and N dividing signal NCLK which are inputted into a phase comparator 6 are branched, respectively, and the exclusive "or" circuit 20 which considers each [ these ] signal as an input is formed. It is used in order to detect whether a phase has this exclusive "or" circuit 20 in a lock condition, or the phase of M dividing signal MCLK and N dividing signal NCLK has gathered. When the phase of M dividing signal MCLK and N dividing signal NCLK has shifted, the period when the logical level of both signals differs arises. In this period, an exclusive "or" circuit 20 outputs the signal of "H" level, and, on the other hand, outputs the signal of "L" level to the period whose logical level of both corresponds. Therefore, conventionally, it had the signal of "H" level from an exclusive "or" circuit 20, and lock-off was detected. Furthermore, it measured conventionally using the external clock which has a small period compared with that period from this exclusive "or" circuit 20, the signal period of phase shifts, i.e., amount, of "H" level outputted, and using for control of the circuit using the output of the PLL circuit 2 or the PLL circuit 2 was also performed.

[0006] Incidentally, since loop control acts so that the frequency and phase of both inputs of a phase comparator 6 may be in agreement, the PLL circuit 2 shown in drawing 3 is controlled to become fM=fN, i.e., fR/M=fOUT/N, in a lock condition. That is, an output signal OCLK serves as a frequency which becomes fOUT=N/MxfR, and the signal changed into the signal fR N/M twice the frequency of an input reference is outputted from VCO14. Here, by changing N and M, the signal of various frequencies can be acquired and the circuit which applies this and is called a frequency synthesizer is

realized.

## EFFECT OF THE INVENTION

[Effect of the Invention] according to the phase lock detector of this invention -- counting -- a period generation circuit -- the input-reference signal to a PLL circuit -- being based -- counting -- a period signal -- generating -- an output signal counter -- counting -- counting defined by the period signal -- the wave number of the output signal outputted to a period from a PLL circuit is counted. A lock judging circuit judges whether it is a phase lock condition for this output counted value as compared with criteria counted value. That is, the signal inside a PLL circuit generated in-between is not used for a basis phase lock detector at all using the input-reference signal to a PLL circuit, and the output signal outputted as the final result from a PLL circuit. Thereby, the phase lock detector of this invention can be applied also to the integrated PLL circuit, an accurate phase lock detection means is offered to the PLL circuit integrated with the configuration which does not include a phase lock detection means especially in the interior, and the effectiveness of expanding the use range of the PLL circuit is brought about.
[0029] The phase lock detector of this invention not needing the external clock whose frequency's was stable in the actuation, and criteria counted value are beforehand defined based on the design parameter of a PLL circuit etc., by not being dependent on the stability of an input-reference signal, are very easy to constitute and, moreover, effective in it being stable and an accurate phase lock detector being offered.

## TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] In the conventional phase lock detector mentioned above, two signals which are inputted into an exclusive "or" circuit 20 and compared with it turn into two signals which are inputted into a phase comparator 6 and compared. Now, in order to attain the miniaturization of the equipment using the PLL circuit 2, there are not few cases where integrate on a semi-conductor substrate, or the whole PLL circuit 2 or the part which contains a phase comparator 6 at least is offered with the gestalt contained in one package, and this is used as components which constitute equipment. In components-izing of such a PLL circuit 2, although a part of range included to the phase lock detector according to the application may be used as elegance, since the need of detecting especially a phase lock is a low application, there are some which are offered as smaller components only in the part which does not include a phase lock detector. however, generally the PLL circuit module constituted so that the phase lock detector of this latter might not be included takes out outside two signals both inputted into a phase comparator 6 -- as -- it is not constituted. Therefore, there was a problem that the conventional phase lock detector could also be prepared by external, and that use range was limited to the PLL circuit module which does not include this phase lock detector.

[0008] Moreover, with the configuration of the phase lock detector using the conventional exclusive "or" circuit 20, when lock-off needed to be evaluated quantitatively, there was also a problem that the external clock whose frequency was stable was needed apart from the clock for actuation of PLL circuit 2 the very thing.
[0009] It was not made in order that this invention might cancel the above-mentioned trouble, and it makes it possible to perform phase lock detection also to the PLL passive circuit elements which do not include a phase lock detector, and aims at offering the phase lock detector which moreover does not need a special external clock.

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MEANS

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[Means for Solving the Problem] The phase lock detector concerning this invention is used for the phase-locked loop circuit which generates the output signal of the frequency which has a predetermined frequency-conversion ratio to the frequency of an input-reference signal. The output signal counter which is the phase lock detector which detects the phase lock of the phase-locked loop circuit concerned, and carries out counting of the wave number of said output signal outputted from said phase-locked loop circuit, counting of said output signal counter -- counting which defines a period -- counting which generates a period signal based on said input-reference signal -- with a period generation circuit said frequency-conversion ratio and said counting -- it has the lock judging circuit which judges said phase lock based on the difference between the criteria counted value beforehand defined based on a period, and the output counted value of said output signal counter.
[0011]
[Embodiment of the Invention] Next, the operation gestalt of this invention is explained with reference to a drawing. Drawing 1 is the block diagram of the outline of the frequency synthesizer using PLL which is the gestalt of operation of this invention. The input-reference signal RCLK32 is inputted into the integration PLL circuit 30 constituted including the PLL circuit 2, and it outputs the output signal OCLK34 which has the frequency fOUT which doubled this frequency fR N/M. This integration PLL circuit 30 does not need to have the terminal for taking out the signal in that interior. the phase lock detector 40 concerning this invention -- counting -- it is constituted including the period generation circuit 42, the output signal counter 44, and the lock detector 46. The lock judging circuit 46 includes the counted value comparator circuit 48 which compares the criteria counted value set up beforehand with the output counted value outputted from the output signal counter 44. About a detail of operation, it mentions later using more detailed drawing. Here, only the big description of a basis phase lock detector is explained using drawing 1 . The input-reference signal RCLK32 with which the big description of the phase lock detector 40 is inputted into the integration PLL circuit 30, and the signal generated in-between in the integration PLL circuit 30 interior, using the output signal OCLK34 with which it is finally generated by the integration PLL circuit 30, and is outputted as a main input signal are in the point which is not needed.
[0012] Drawing 2 is the block diagram shown to the block configuration inside the integration PLL circuit 30, in order to explain actuation of the gestalt of this operation.

Dividing of the input-reference signal RCLK32 of the frequency fR from the outside is carried out with the M counting-down circuit 64, and M dividing signal MCLK66 which has the frequency fM of 1/M of an input-reference signal is generated.
[0013] Moreover, although the output signal OCLK34 which finally has a frequency fOUT is outputted from the integration PLL circuit 30, this OCLK34 branches in the integration PLL circuit 30 interior, and one of them is inputted into the N counting-down circuit 68. The N counting-down circuit 68 carries out dividing of the OCLK, and generates N dividing signal NCLK70 which has the frequency fN of the 1-/N.
[0014] M dividing signal MCLK66 and N dividing signal NCLK70 which were generated in this way are inputted into a phase comparator 72. PLL controls so that the phase of two input signals to this phase comparator 72 gathers. Incidentally, the conventional phase lock detector mentioned above used the property of this PLL of being controlled to have the frequency and phase with two same inputs to this phase comparator 72. On the other hand, since the phase lock detector 40 does not use this property, it does not need to output MCLK66 or NCLK70 which the integration PLL circuit 30 generates in that interior.
[0015] A phase comparator 72 detects the phase contrast of MCLK66 and NCLK70 which were inputted, and outputs the error signal according to the phase contrast. The charge pump 74 changes and outputs the error signal from a phase comparator 72 to "H" level and "L" level and three values of high impedance. A low pass filter 76 graduates the output signal of the charge pump 74, and controls VCO78 by the dc component. VCO78 outputs the output signal OCLK which has the oscillation frequency fOUT according to the direct current voltage of the output of a low pass filter 76.
[0016] Since loop control acts so that the frequencies fM and fN of both inputs of a phase comparator 72 may be in agreement as already stated, it is set to fOUT= (N/M) and fR. That is, the signal changed into the signal fR N/M twice the frequency of an input reference is outputted from VCO78, and the frequency synthesizer which can acquire the signal of various frequencies is realized by changing N and M.
[0017] Now, actuation of the phase lock detector 40 is explained below. RCLK32 inputted into the integration PLL circuit 30 branches -- having -- counting of the phase lock detector 40 -- it is inputted into the period generation circuit 42. counting -- the period generation circuit 42 is constituted including a counter, and generates the measurement period signal pulse which has the time amount length WREF which corresponds the predetermined twice of the period based on RCLK. For example, it can be set as WREF=1sec extent to fR=14MHz. This measurement period signal pulse is supplied to the output-signal counter 44 as an enable signal.
[0018] The time amount width of face WREF is set up more greatly than periodic tauOUT of an output signal OCLK. That is, it is set up so that it may become WREF=kOUT-tau OUT (kOUT> 1) by making kOUT into a proportionality constant. Here, the accuracy of measurement improves, so that WREF is so large that [ that is, ] kOUT is large since the accuracy of measurement of the phase shift of tauOUT serves as 2 pi/kOUT [rad] about.
[0019] When a measurement period signal pulse is in enabling state, the output-signal counter 44 counts the wave number of the output signal OCLK inputted from the integration PLL circuit 30, and outputs the counted value (output counted value COUT).
[0020] Output counted value COUT which the output signal counter 44 counted is

inputted into the counted value comparator circuit 48 in the lock judging circuit 46. The wave number of the output signal generated between measurement period signal pulse width WREF(s) in the phase lock condition of this integration PLL circuit 30 is beforehand set to the counted value comparator circuit 48 as criteria counted value CREF. The counted value comparator circuit 48 compares this criteria counted value CREF with output counted value COUT actually measured by the output signal counter 44.

[0021] the case of COUT>CREF -- the ratio of the frequency of OCLK, and the frequency of RCLK -- it means that correspond when fOUT/fR is larger than N/M, that is, the phase of OCLK progresses to RCLK. On the other hand, it means that the phase of OCLK is overdue to RCLK in COUT<CREF. In a phase lock condition, frequency-ratio fOUT/fR=N/M is realized and this is distinguished from becoming COUT=CREF. Thus, the counted value comparator circuit 48 can judge the size relation between COUT and CREF, and the lock judging circuit 46 can detect the existence of the phase shift of RCLK and OCLK based on the judgment result. Although this phase shift may always be produced, a little gap is easily corrected by the loop control by PLL. If the difference between COUT and CREF becomes more than how much, the lock judging circuit 46 will have the conditions of whether to judge with lock-off set up, will perform the judgment of a phase lock condition or a lock OFF state based on the criterion, and it outputs the result.

[0022] If CREF set as the counted value comparator circuit 48 has fixed frequency-ratio N/M, it is good at a predetermined fixed value. However, either of the division ratios M and N of the M counting-down circuit 64 of the integration PLL circuit 30 and the N counting-down circuit 68 is constituted by adjustable, and when frequency-ratio N/M is adjustable, CREF is also changed according to it. This modification can be constituted so that user actuation and frequency-ratio change actuation of the integration PLL circuit 30 may be interlocked with and it may be automatically carried out from the exterior of the phase lock detector 40.

[0023] The value of CREF set as the counted value comparator circuit 48 is given by WREF-fOUT. However, fOUT which appears in this formula is not the actual frequency of OCLK outputted from the integration PLL circuit 30 but that desired value. That is, fOUT here is equivalent to -(N/M) fR. Table 1 is a table showing the example of CREF set to the counted value comparator circuit 48. In a table, the left column is fOUT as a target frequency of the output signal OCLK mentioned above, and the right column is a frequency setting value which is CREF corresponding to each fOUT in the case of being WREF=1sec. This frequency set point CREF is expressed in hexadecimals corresponding to the data format on the memory with which the counted value comparator circuit 48 is equipped.

[Table 1]

| PLL出力信号 | 周波数設定値 (HEX) |
|---|---|
| 10kHz | 2710 (HEX) |
| 100kHz | 186A0 (HEX) |
| 1MHz | F4240 (HEX) |
| 10MHz | 989680 (HEX) |

[0024] now, counting -- since the period generation circuit 42 determines the time

amount width of face WREF using the counter which operates synchronizing with RCLK, if the frequency of RCLK is changed, WREF will also interlock and change to it. the actual period to which RCLK may be changed in tauREF here, and kREF -- a proportionality constant, then actual counting -- the time amount width of face of a period signal pulse can be expressed with a degree type.

[0025]

WREF=kREF-tau REF ..... (1)

WREF-fOUT which gives the value of CREF on the other hand as mentioned above is equivalent to a degree type.

[0026]

(N/M) WREF-fR ..... (2)

(2) In a formula, WREF and fR are the actual values which may be changed, respectively. (2) When (1) type is substituted for a formula, WREF is eliminated and it takes into consideration that it is fR=1-/tauREF, as for CREF, it turns out that it is expressed in the format of not being influenced by RCLK of fluctuation, like a degree type.

[0027]

CREF= (N/M) and kREF ..... It does not depend on an actual measurement for the value of CREF set to (3) <BR>, i.e., a counted value comparator circuit, from this, but it turns out that it is good by the constant called for from the design parameter of a circuit. [48 ] That is, this equipment is easy to constitute at the point that what is necessary is just to set beforehand CREF which is not influenced by RCLK of fluctuation as the counted value comparator circuit 48, and, moreover, the precision of a judgment of the condition of a phase lock is secured also by such easy configuration.

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## DESCRIPTION OF DRAWINGS

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[Brief Description of the Drawings]

[Drawing 1] It is the block diagram of the outline of the frequency synthesizer using PLL which is the gestalt of operation of this invention.

[Drawing 2] It is the block diagram of the frequency synthesizer which is the gestalt of operation of this invention, and is the block diagram shown to the configuration inside an integration PLL circuit.

[Drawing 3] It is the block block diagram of a phase-locked loop circuit known conventionally.

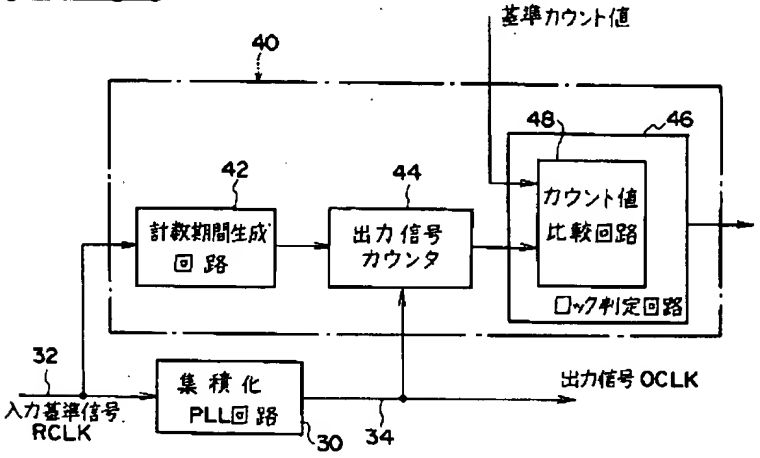
[Drawing 4] It is the block block diagram of the PLL circuit equipped with the conventional phase lock detector.

[Description of Notations]

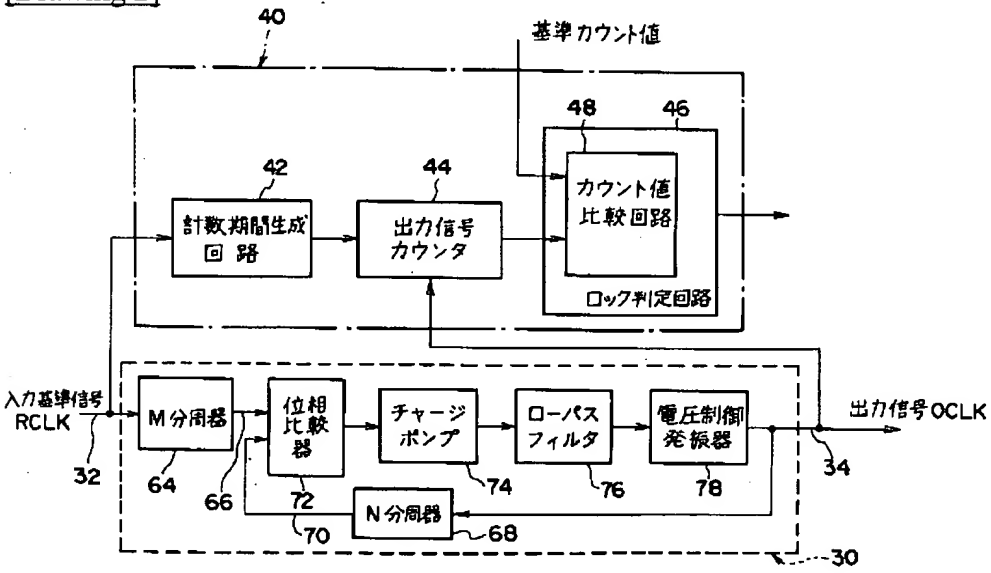
30 an integration PLL circuit and 32 voltage controlled oscillator. An input-reference signal and 34 An output signal and 40 A phase lock detector and 42 counting -- a period generation circuit and 44 An output signal counter and 46 A lock judging circuit and 48 A counted value comparator circuit and 64 M counting-down circuit and 66 M dividing signal and 68 N counting-down circuit and 70 N dividing signal and 72 A phase comparator and 74 A charge pump and 76 A low pass filter and 78

## DRAWINGS

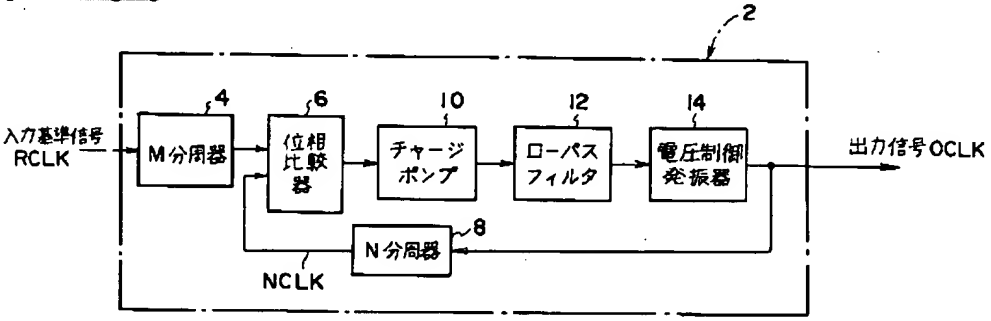
[Drawing 1]



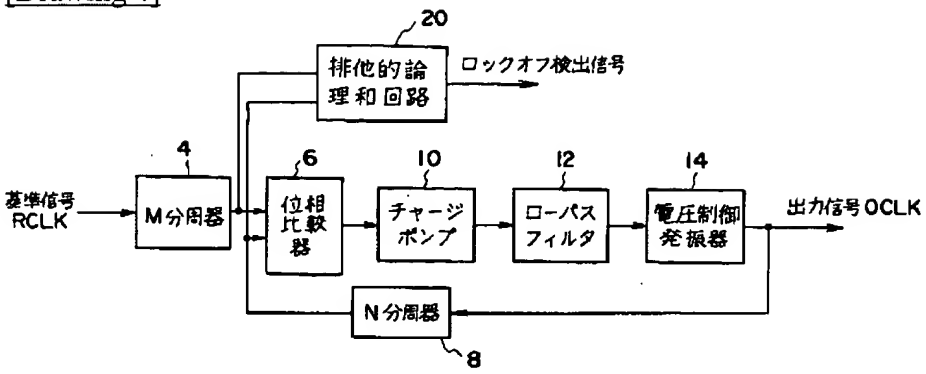

[Drawing 2]




[Drawing 3]



[Drawing 4]


20
排他的論理和回路
ロックオフ検出信号
4
6
10
12
14
基準信号 RCLK
M分周器
位相比較器
チャージポンプ
ローパスフィルタ
電圧制御発振器
出力信号 OCLK
N分周器
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